

## CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

- 1           1.       An analog front end for a digital subscriber line data communication  
2 system, comprising:  
3           a line driver for transmitting a data signal over a local loop;  
4           a digital to analog converter having an output connected to an input of the line  
5 driver, the digital to analog converter also having a data input for receiving a digital data  
6 signal and a clock input for receiving a clock signal; and  
7           a data signal supervisor circuit having a first input configured to receive the data  
8 signal and a second input configured to receive the clock signal, the supervisor circuit  
9 having comparison circuitry for logically comparing a first value of the data signal in  
10 relation to a signal change of the clock signal to a second value of the data signal in  
11 relation to a previous signal change of the clock signal and asserting a transmit control  
12 output signal if the first value of data signal is the same as the second value of the data  
13 signal.
  
- 1           2.       The analog front end of claim 1, further comprising:  
2           a clock detector circuit having an input configured to receive the clock signal, the  
3 clock detector circuit further including frequency detection circuitry configured to assert a  
4 reset signal in response to the frequency of the clock signal.
  
- 1           3.       The analog front end of claim 1, further comprising:  
2           a control circuit having a reset input configured to receive a reset signal from the  
3 clock detector, the control circuit configured to reinitialize the digital subscriber line data  
4 communication system in response to the reset signal.
  
- 1           4.       The analog front end of claim 3, wherein the control circuit includes  
2 circuitry for commanding the digital to analog converter to disable an output signal.

1           5.       The analog front end of claim 1, wherein the comparison circuitry includes  
2       a counter circuit configured to count a predetermined number of clock signal cycles  
3       wherein the data signal remains unchanged.

1           6.       The analog front end of claim 5, wherein the comparison circuitry further  
2       comprises Exclusive Or logic having an input that is indicative of the logical comparison  
3       of a first value of the data signal with a second value of the data signal, the Exclusive Or  
4       logic being in communication with an input of the counter circuit.

1           7.       An analog front end for a digital subscriber line data communication  
2       system, comprising:  
3               means for transmitting a data signal;  
4               means for converting a digital input signal into an analog representation of the  
5       digital input signal;  
6               means for detecting an at least one data signal anomalous condition; and  
7               means for asserting an at least one transmit control output signal in response to the  
8       at least one data signal anomalous condition.

1           8.       The analog front end of claim 7, wherein the means for transmitting a data  
2       signal receives a digital data stream from a delta-sigma modulator.

1           9.       The analog front end of claim 7, wherein the means for detecting an at  
2       least one data signal anomalous condition is performed by monitoring a digital data  
3       stream.

1           10.      The analog front end of claim 9, wherein the digital data stream comprises  
2       a data signal and a clock signal.

1           11.      The analog front end of claim 10, wherein the means for detecting an at  
2       least one data signal anomalous condition is performed by a data supervisor.

1           12.     The analog front end of claim 10, wherein the means for detecting an at  
2     least one data signal anomalous condition is performed by a clock detector.

1           13.     A method for monitoring data transmissions in an analog front end,  
2     comprising:  
3                 comparing consecutive values of a digital data signal in relation to a clock signal;  
4     and  
5                 identifying a transmission error condition if there is no substantial change in the  
6     consecutive values of the digital data signal within a predetermined number of clock  
7     signal cycles.

1           14.     The method of claim 13, further comprising:  
2                 monitoring the frequency of the clock signal; and  
3                 generating a reset signal if the frequency of the clock signal falls below a  
4     predetermined value.

1           15.     A transmission signal integrity supervisor, comprising:  
2                 a clock detector configured to receive a clock signal input and generate a first  
3     output signal in response to an at least one clock signal input anomalous condition; and  
4                 a data supervisor configured to receive a digital data stream and generate a second  
5     output signal in response to an at least one digital data stream anomalous condition.

1           16.     The signal integrity supervisor of claim 15, wherein the first output signal  
2     is a reset signal.

1           17.     The signal integrity supervisor of claim 15, wherein the second output  
2     signal is a power down signal.

1           18.     The signal integrity supervisor of claim 15, wherein the data supervisor  
2     receives a digital data stream from a delta-sigma modulator.

1           19.     The signal integrity supervisor of claim 15, wherein the clock detector  
2 comprises a first monostable circuit and a second monostable circuit.

1           20.     The signal integrity supervisor of claim 19, wherein the clock detector  
2 further comprises:  
3           a current mirror; and  
4           a resistor – capacitor combination having a resistance and a capacitance value  
5 respectively, selected such that the first output signal triggers in response to a clock signal  
6 input that falls below a minimum frequency.

1           21.     The signal integrity supervisor of claim 15, wherein the data supervisor  
2 comprises:  
3           a comparator; and  
4           a maximum number counter.

1           22.     The signal integrity supervisor of claim 21, wherein the comparator is  
2 configured to compare a data value from a previous clock cycle with a current data value  
3 and to generate a reset signal in response to consecutive data levels that vary.

1           23.     The signal integrity supervisor of claim 21, wherein the maximum number  
2 counter is configured to increment upon detecting a clock cycle until it receives the reset  
3 signal from the comparator.

1           24.     The signal integrity supervisor of claim 23, wherein the maximum number  
2 counter is configured to generate an output signal upon reaching a maximum count.

1           25.     The signal integrity supervisor of claim 24, wherein the maximum number  
2 counter comprises a 4-bit asynchronous counter.

1           26.    A circuit, comprising:  
2                means for monitoring a digital data stream; and  
3                means for generating an output signal in response to an anomalous condition in  
4   the digital data stream.

1           27.    The circuit of claim 26, wherein the anomalous condition in the digital  
2   data stream would create a direct current (DC) transmit signal.

1           28.    The circuit of claim 26, wherein the means for monitoring a digital data  
2   stream comprises a signal integrity supervisor.

1           29.    The circuit of claim 28, wherein the signal integrity supervisor comprises a  
2   clock detector and a data supervisor.

1           30.    The circuit of claim 28, wherein the means for generating an output signal  
2   is responsive to a digital data stream having a number of consecutive data values of equal  
3   magnitude wherein the number of consecutive data values reaches a predetermined  
4   maximum value.

1           31.    The circuit of claim 28, wherein the means for generating an output signal  
2   is responsive to a digital data stream having a clock signal that falls below a  
3   predetermined minimum frequency.

1           32.    A transmission unit, comprising:  
2                a signal integrity supervisor configured to generate a response to a digital data  
3   stream having an anomalous condition.

1           33.    The transmission unit of claim 32, wherein the digital data stream  
2   anomalous condition is a clock signal frequency that falls below a predetermined  
3   minimum value.

1           34.     The transmission unit of claim 32, wherein the digital data stream  
2     anomalous condition is a data signal having a corresponding data value that does not vary  
3     for a predetermined maximum number of clock cycles.

1           35.     A method for preventing a transmission unit from forwarding a transmit  
2     signal that may result in a DC flow condition, comprising:  
3         monitoring a data signal;  
4         generating a first signal in response to a data signal condition;  
5         monitoring a clock signal; and  
6         generating a second signal in response to clock signal condition.

1           36.     The method of claim 35, wherein the data signal is provided by a delta-  
2     sigma modulator.

1           37.     The method of claim 35, wherein the step of monitoring a data signal is  
2     performed with a digital comparator.

1           38.     The method of claim 35, wherein the first signal is a power down signal.

1           39.     The method of claim 38, wherein the power down signal is generated in  
2     response to a data signal having an unchanging value.

1           40.     The method of claim 39, wherein the power down signal is generated by  
2     an asynchronous counter that reaches a maximum value.

1           41.     The method of claim 35, wherein the second signal is a reset signal.

1           42.     The method of claim 41, wherein the reset signal is generated in response  
2     to a clock signal having a frequency that fails to exceed a predetermined minimum value.

- 1           43.     The method of claim 42, wherein the reset signal is generated by a
- 2     monostable circuit.